

A 56.1Gb/s NRZ Modulated 850nm VCSEL-Based Optical Link

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Abstract: We report a directly modulated 850nm VCSEL-based optical link operating at 56.1Gb/s (BER < 1E-12). This is the highest modulation rate for a VCSEL-based link of any wavelength. An open eye is obtained at 60Gb/s.

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1. Introduction

High Performance Computing, Data Centers, and the Internet in general are driving the demand for high bandwidth interconnects. Already, serial data rates of 25.78Gb/s (Ethernet, Infiniband) and 28.05Gb/s (Fibre Channel) have been standardized with directly modulated 850nm VCSELs as part of the solution. It is anticipated that there will be proposals for the next generation of these standards with serial data rates above 50Gb/s. In particular, 64G Fiber Channel is likely to be 56.1Gb/s. For VCSELs, the highest serial data rates demonstrated, error free (commonly defined as BER < 1E-12), thus far are 55Gb/s equalized [1] and 44Gb/s unequalized [2] at 850nm, 49Gb/s at 980nm (-10°C) [3], 40Gb/s at 1100nm [4], and 35Gb/s at 1550nm [5]. It is important to note that many of the record VCSEL modulation results [2-5] are obtained with test equipment driving the laser and test equipment for the O/E conversion (e.g. a reference photodiode or receiver); here we report a complete link: laser driver + VCSEL to photodiode + RX IC. In this paper, we demonstrate that advanced VCSELs, combined with fast circuits and equalization, can operate above 50Gb/s and should continue to be part of the solution for future high speed serial links. To the best of our knowledge, this reported data rate of 56.1Gb/s is the highest data rate for any VCSEL link, regardless of wavelength.

2. Experiment

The full link is comprised of a driver chip with two tap feed forward equalization (FFE) wirebonded to an 850nm VCSEL and a GaAs PIN photodiode wirebonded to a receiver IC, also with two tap FFE. The driver and receiver chips are fabricated in the IBM BiCMOS8HP process and exclusively utilize the npn SiGe bipolar transistors for all of the active circuits. Figure 1 shows a block diagram of the link. The driver IC is similar to a previously published design [6], but with a 50 Ohm output impedance and a re-tuned output equalizer. The 50 Ohm output impedance provides faster rise and fall times compared to the 100 Ohm design in [1], albeit at lower modulation efficiency. The receiver is an updated and improved version of the design in [6]. The ICs and corresponding OEs are separately packaged on a printed circuit board with short (~0.5") 50 Ohm transmission lines to SMP coaxial connectors. All active components on the circuit boards are wirebonded as can be seen in Figure 2. The differential outputs of the driver chip are wirebonded to separate VCSELs: the optical output of one VCSEL is used, while the other VCSEL is a dummy to balance the load at the driver output. In a product design, the dummy load VCSEL would be straightforwardly replaced by an on-chip load or omitted entirely to save power.

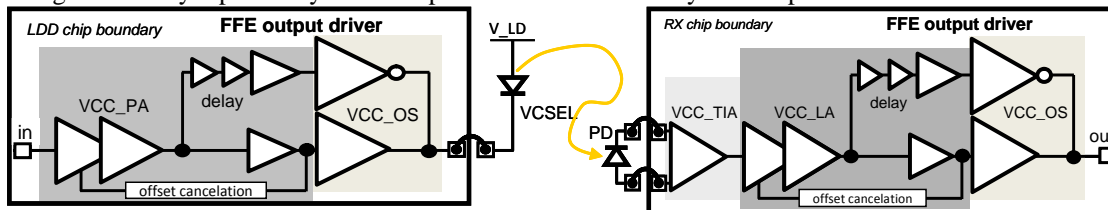


Figure 1. Block Diagram of full optical link showing internal elements of the driver and receiver ICs.

The VCSEL used in this work was grown on an n-type substrate by low pressure MOCVD and consists of a lower n-type DBR, a four quantum well active region, and a p-type upper DBR. The VCSEL was fabricated with a single anode contact on the top and a cathode contact through the substrate. Parasitic

capacitance was minimized by incorporating a thick dielectric coating under the anode bond pad connection. The approximately $7\ \mu\text{m}$ current and optical emission aperture is formed by steam oxidation. The VCSEL has a threshold current of approximately $600\ \mu\text{A}$, slope efficiency of $0.3\ \text{W/A}$, and series resistance of $100\ \text{Ohms}$. The measured 3dB optical bandwidth is approximately $24\ \text{GHz}$. The photodiode, described in [7], has a $25\ \mu\text{m}$ active diameter and a 3dB electrical bandwidth of $22\ \text{GHz}$ at $-3\ \text{V}$.

3. Results

The full link is characterized from 40 to $56.1\ \text{Gb/s}$ using PRBS7. The pattern generator is an SHF 12103A and the error detector is an SHF 11100A. The pattern generator output is connected to the Tx printed circuit board differentially through a pair of $6''$ cables. The output amplitude is set for $430\ \text{mV}$ peak-to-peak single-ended. The receiver differential output is split with one side connected to the error detector and the other connected to an oscilloscope; both cables are $6''$ long. For bathtub measurements at $56\ \text{Gb/s}$, both Rx outputs were connected differentially to the error detector. The VCSEL output and photodiode input are coupled by lensed fiber probes ($\sim 80\%$ coupling efficiency Tx, $\sim 100\%$ coupling Rx).

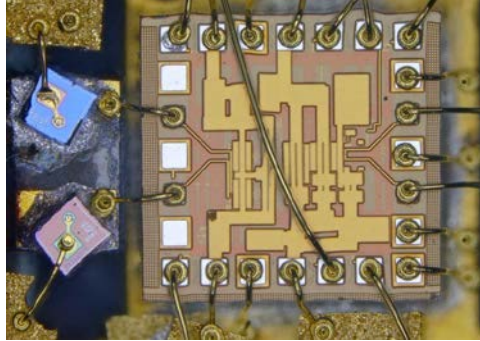


Figure 2. Picture of the SiGe driver IC showing wire bond connections to the VCSEL and package.

The link is comprised of either $5\ \text{m}$ of $50/125\ \text{OM2}$ grade fiber or $2\ \text{m}$ of $26/125$ fiber. The specific fiber type is not important for this essentially back-to-back demonstration. Error-free operation (defined as $\text{BER} < 1\text{E-}12$) is obtained up to $56.1\ \text{Gb/s}$. At $56.1\ \text{Gb/s}$, the short term BER was low enough to permit several Tbits to be transmitted error-free at one time ($\text{BER} < 6\text{E-}13$). Figure 3 shows the eye diagrams and bathtub curves for 3 data rates: 40 , 50 , and $56.1\ \text{Gb/s}$ using the same link settings. The VCSEL bias is $8.1\ \text{mA}$ and the photodiode bias is $-7\ \text{V}$. The transmitter temperature is 25°C . The received photocurrent is $522\ \mu\text{A}$ which corresponds to $950\ \mu\text{W}$ average power. Over- and under-shoot from the receiver FFE circuitry is observable in the eyes. At $40\ \text{Gb/s}$, the eye opening is $0.57\ \text{UI}$, or $14.3\ \text{ps}$, which is comparable to the $0.58\ \text{UI}$ obtained in [6] using conditions optimized for $40\ \text{G}$. At $56.1\ \text{Gb/s}$, there is $2.0\ \text{ps}$ ($0.11\ \text{UI}$) of eye opening at $\text{BER}=1\text{E-}12$. The eye opening from the test equipment back-to-back is $0.68\ \text{UI}$ at $56\ \text{Gb/s}$. The total link power dissipation is $1.33\ \text{W} = 682\ \text{mW Tx} + 648\ \text{mW Rx}$, corresponding to energy consumption of $23.7\ \text{pJ/bit}$ for the system at $56.1\ \text{Gb/s}$, with the VCSEL itself contributing a low $245\ \text{fJ/bit}$.

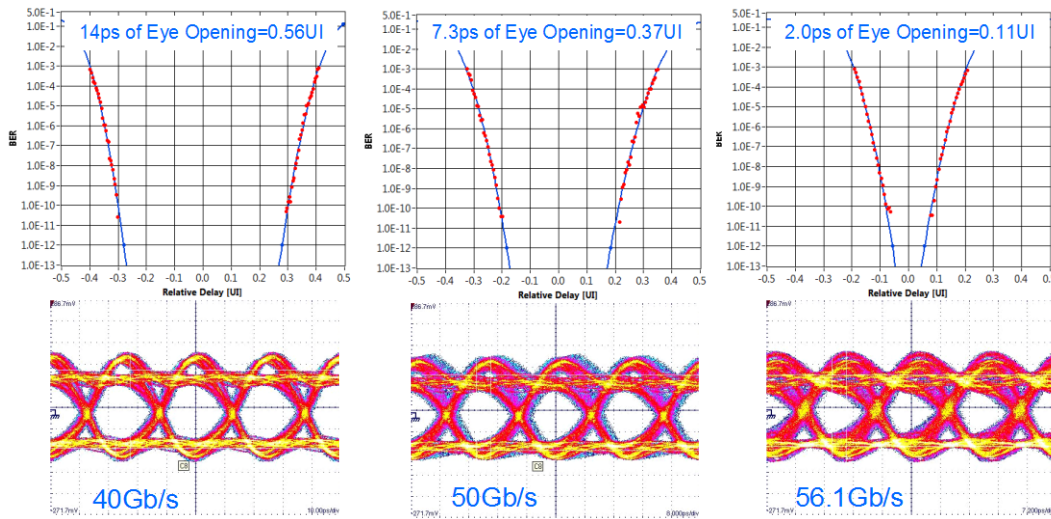


Figure 3. Link Eye Diagrams and Bathtub curves for three data rates: 40, 50, and 56.1Gb/s (left to right). For the eye diagrams, vertical scale is 56mV/div and the horizontal scales are 10, 8, and 7.2ps/div, respectively.

Using a dual Dirac model, the deterministic and random jitter are extracted from each bathtub curve. The extracted jitter values are (DJ [ps], RJ [fs rms]), (0.69, 736), (2.56, 721) and (7.44, 597) for 40, 50 and 56.1Gb/s respectively.

Although the error detector operates only to 56Gb/s, the pattern generator can operate to 60Gb/s with increased jitter. An open eye diagram was obtained from the link at 60Gb/s, see Figure 3.

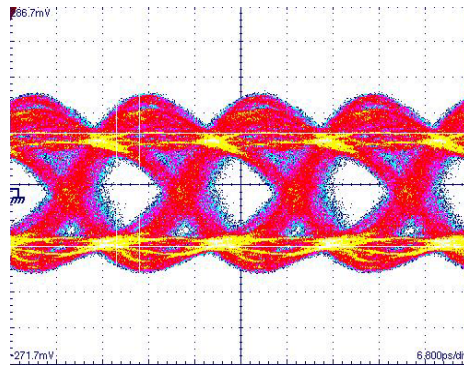


Figure 4. Link Eye Diagram at 60Gb/s showing an open eye.

3. Conclusion

We have demonstrated a full optical link, IC to IC, with margin at 56.1Gb/s, the highest serial bit rate yet published for any NRZ directly-modulated VCSEL. This performance is made possible by a high bandwidth VCSEL and by the use of fast ICs with transmitter equalization which allows the total link to exceed the speed capabilities of the individual OE devices. Additionally, the use of 850nm components, the industry standard, combined with a readily available BiCMOS process offering enables a straightforward path to commercialization and compatibility with high-bandwidth OM3 and OM4 grade fiber. Equalized links using direct NRZ modulation are a convenient and viable path forward to satisfy the needs for future higher serial data rates without having to resort to complicated coding or modulation schemes or forward error correction. With higher speed test equipment, and ever improving circuits and optical devices, operation at rates >60Gb/s are certainly possible within the next several years.

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